TMD3782

Color Light-to-Digital Converter with Proximity Sensing

General Description

The TMD3782x device will perform color temperature measurement, ambient light sensing (ALS) and proximity detection with background light rejection. The device detects light intensity under a variety of lighting conditions and through a variety of attenuation materials, including dark glass. The proximity detection feature allows a large dynamic range of operation for accurate distance detection, such as in a cell phone when the user positions the phone close to their ear. IR LED sink current is factory trimmed to provide consistent proximity response without requiring customer calibrations. An internal state machine provides the ability to put the device into a low power state between proximity and RGBC measurements providing very low average power consumption.

The color sensing feature is useful in applications such as backlight control, solid state lighting, reflected LED color sampler, or fluorescent light color temperature detection. The integrated IR blocking filter makes this device an excellent ambient light sensor, color temperature monitor, and general purpose color sensor.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TMD3782, Color Light-to-Digital Converter with Proximity Sensing are listed below:

Figure 1:
Added Value of Using TMD3782

Benefit	Feature

• Single Device Integrated Optical Solution	• RGB, Ambient Light Sensor (ALS) and Proximity Support
	  • Power Management Features
	  • I^2C Fast Mode Interface Compatible
	  • Integral IR LED
	  • Small 8 lead optical module

• Color Temperature and Ambient Light Sensing	• UV / IR blocking filters • Programmable Gain & Integration Time • 1,000,000:1 Dynamic Range
• Equal Response to 360º Incident Light	• Circular Segmented RGBC Photodiode
• Ideal for Operation Behind Dark Glass	• Very High Sensitivity

Benefit	Feature
• Proximity Detection with Integrated IR LED	• Background Ambient Light Rejection • Factory Trimmed, Consistent Response • Programmable Current Sink for IR LED Drive

Applications

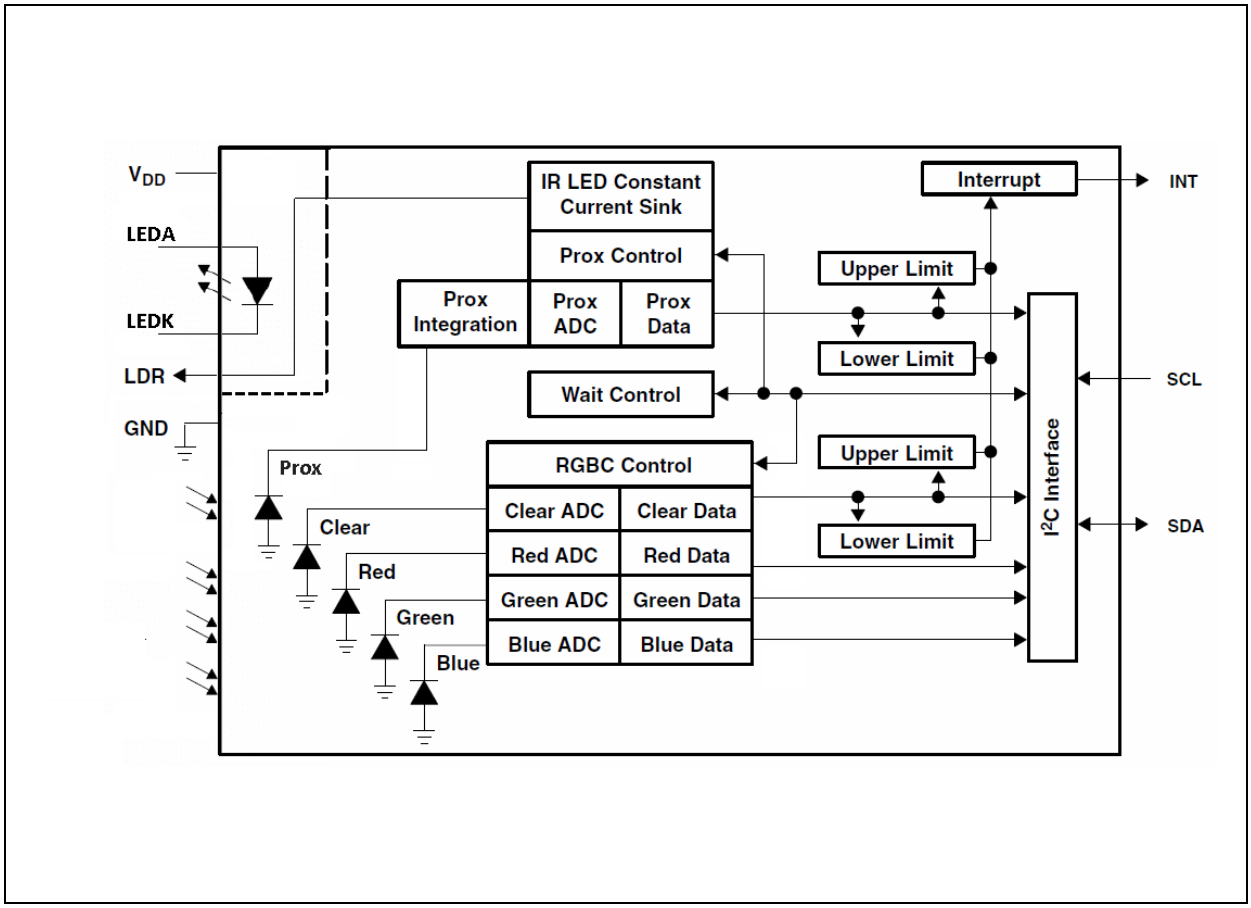
The TMD3782 applications include:

- Ambient Light Sensing
- Color Temperature Sensing
- Cell Phone Touch Screen Disable
- Mechanical Switch Replacement
- Industrial Process Control
- Medical Diagnostics

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
TMD3782 Block Diagram



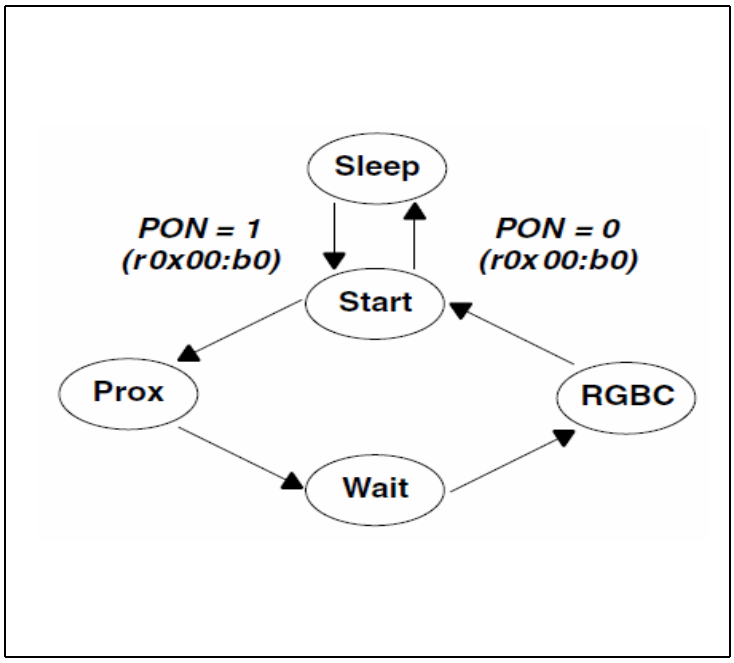
Detailed Description

The TMD3782 is a digital color light sensor device containing four analog-to-digital converters (ADCs) that integrate currents from photodiodes. Multiple photodiode segments for red, green, blue, and clear are geometrically arranged to reduce the reading variance as a function of the incident light angle. Integration of all color sensing channels occurs simultaneously. Upon completion of the conversion cycle, the result is transferred to the corresponding data registers. The transfers are double-buffered to ensure that the integrity of the data is maintained. Communication with the device is accomplished through a fast (up to 400 kHz), two-wire I^2C serial bus for easy connection to a microcontroller or embedded controller.

The TMD3782 provides a separate pin for level-style interrupts. When interrupts are enabled and a pre-set value is exceeded, the interrupt pin is asserted and remains asserted until cleared by the controlling firmware. The interrupt feature simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity or proximity value. An interrupt is generated when the value of a clear channel or proximity conversion equals or exceeds either an upper or lower threshold. In addition, a programmable interrupt persistence feature allows the user to determine how many consecutive samples must equal or exceed the threshold to trigger an interrupt. Interrupt thresholds and persistence settings are configured independently for both the clear channel and proximity sensors.

Proximity detection is done using a dedicated proximity photodiode centrally located beneath an internal lens, an internal LED, and a driver circuit. The driver circuit requires no external components and is trimmed to provide a calibrated proximity response. Customer calibrations are usually not required. The number of proximity LED pulses can be programmed from 1 to 255 pulses, providing a 2000:1 contiguous dynamic range. Background ambient light is subtracted from the proximity reading to improve accuracy in all lighting conditions.

A state machine controls the functionality. Enabling bits independently determine whether the Proximity, Wait or RGBC / ALS functions are performed. Average power consumption is managed via control of variable endurance low power wait cycles. Once initiated the state machine will run continuously until disabled.



Pin Assignment

The TMD3782 pin assignments are described below.

Figure 3:
Pin Diagram

Package Module - 8 (Top View) Package drawing is not to scale.

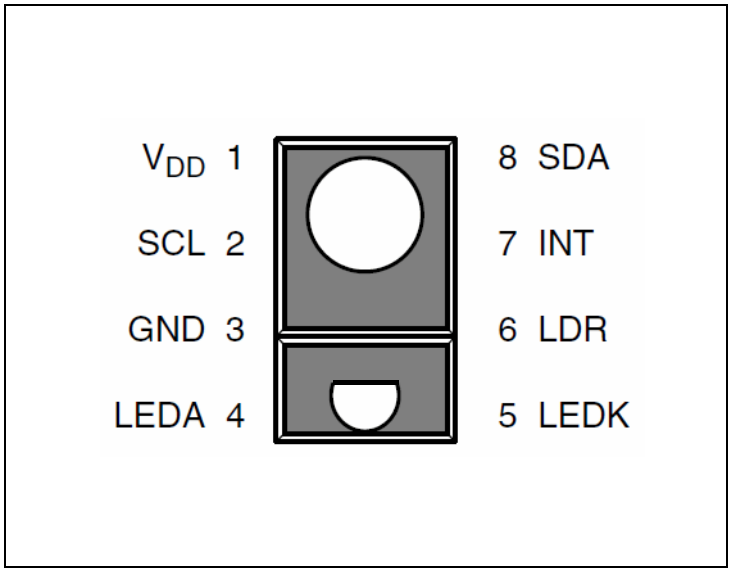


Figure 4:
Pin Description

Pin Number	Pin Name	Typ	Description
1	V_{DD}	PWR	Supply voltage
2	SCL	I	I^2C serial clock input terminal - clock signal for I^2C serial data.
3	GND	GND	Power supply ground. All voltages are referenced to GND.
4	LEDA	PWR	LED anode.
5	LEDK	-	LED cathode. Connect to LDR pin when using internal driver circuit.
6	LDR	-	Proximity IR LED controlled current sink driver.
7	INT	O	Interrupt — open drain (active low)
8	SDA	I/O	I^2C serial data I/O terminal - serial data I/O for I^2C.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Supply Voltage, V_{DD}		3.8	V	All voltages are with respect to GND
Digital I/O Voltage (except LDR)	-0.5	3.8	V	
Max LEDA Voltage (2)		4.8	V	
Max LDR Voltage (3)		4.4	V	
Output Terminal Current (except LDR)	-1	20	mA	
Storage Temperature Range, T_{stg}	-40	85	°C	
ESD Tolerance, JEDEC Specification	±2000		V	JESD22-A11 Class 1C

Note(s) and/or Footnote(s):

1. All voltages are with respect to GND.
2. Maximum 4.8V DC over 7 years lifetime
   Maximum 5.0V spikes with up to 250s cumulative duration over 7 years lifetime
   Maximum 5.5V spikes with up to 10s (=1000*10ms) cumulative duration over 7 years lifetime
3. Maximum voltage with LDR = off

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Supply voltage	2.7	3	3.3	V
T_A	Operating free-air temperature (1)	-30		85	°C

Note(s) and/or Footnote(s):

1. While the device is operational across the temperature range, functionality will vary with temperature. Specifications are stated only at 25°C unless otherwise noted.

Figure 7:
Operating Characteristics, V_{DD}=3V, T_A=25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Supply current	Active - LDR pulses off		235	330	µA
		Wait state		65		
		Sleep state — no I^2C activity		2.5	10	
V_{OL}	INT, SDA output low voltage	3 mA sink current 6 mA sink current	0 0		0.4 0.6	V
I_{LEAK}	Leakage current, SDA, SCL, INT pins		-5		5	µA
I_{LEAK}	Leakage current, LDR pin		-10		10	µA
V_{IH}	SCL, SDA input high voltage	TMD37821 TMD37823	0.7 V_{DD} 1.25			V
V_{IL}	SCL, SDA input low voltage	TMD37821 TMD37823			0.3 V_{DD} 0.54	V

Figure 8:
Optical Characteristics (Clear Channel), V_{DD} = 3V, T_A = 25°C, AGAIN = 16x, ATIME = 0xF6

Parameter	Test Conditions	Clear Channel			Unit
		Min	Typ	Max	
R_e Irradiance responsivity	λ_D = 465 nm (1)	9.4	11.8	14.2	count/ ($\mu W/cm^2$)
	λ_D = 525 nm (2)	12.5	15.6	18.7	
	λ_D = 615 nm (3)	14.6	18.2	21.8	

Figure 9:
Optical Characteristics (RGBC), V_{DD} = 3V, T_A = 25°C

Parameter	Test Conditions	Clear Channel					
		Red Channel		Green Channel		Blue Channel	
		Min	Max	Min	Max	Min	Max
Color ADC count value ratio: Color/Clear	λ_D = 465 nm (1)	0%	15%	10%	42%	70%	90%
	λ_D = 525 nm (2)	4%	25%	60%	85%	10%	45%
	λ_D = 615 nm (3)	80%	110%	0%	14%	5%	24%

Note(s) and/or Footnote(s):

1. The 465 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 465 nm, spectral halfwidth $\Delta\lambda$½ = 22 nm.
2. The 525 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 525 nm, spectral halfwidth $\Delta\lambda$½ = 35 nm.
3. The 615 nm input irradiance is supplied by a AlInGaP light-emitting diode with the following characteristics: dominant wavelength λ_D = 615 nm, spectral halfwidth $\Delta\lambda$½ = 15 nm.

Figure 10:
RGBC Characteristics, V_{DD} = 3 V, T_A = 25°C, AGAIN = 16x, AEN = 1 (unless otherwise noted)

Parameter	Conditions	Channel	Min	Typ	Max	Units
Dark ADC count value	E_e = 0, AGAIN = 60x, ATIME=0xD6 (100ms)		0	1	3	counts
			0		1	counts(1)
ADC integration time step size	ATIME = 0xFF		2.25	2.38	2.53	ms
ADC number of integration steps			1		256	steps
ADC counts per step			0		1023	counts
ADC count value	ATIME = 0xC0 (152.3 ms)		0		65535	counts
Gain scaling, relative to 1× gain setting (2)	AGAIN = 4x AGAIN = 16x AGAIN = 60x		3.8 15 58	4.0 16 60	4.2 17 63	×

Note(s) and/or Footnote(s):

1. Based on typical 3-sigma distribution. Not 100% tested.
2. Clear channel response to a red LED light source with a dominant wavelength (λ_D) of 615 nm and a spectral halfwidth ($\Delta\lambda$½) of 20 nm.

Figure 11:
Proximity Characteristics, V_{DD} = 3 V, T_A = 25°C, PEN = 1 (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
I_{DD} Supply current	LDR pulse on		3		mA
ADC conversion time step size		2.25	2.38	2.53	ms
LED pulse period			14		us
LED pulse width	LED on time		6.3		us
Nominal LED drive current (measured at LDR=0.6V) (1)	PDRIVE = 0 (100%) PDRIVE = 1 (50%) PDRIVE = 2 (25%) PDRIVE = 3 (12.5%)		100 50 25 12.5		mA
Proximity offset, no target (2), (3)	Pulses: 8 PDRIVE = 0 (100%)	100	165	230	counts
Proximity response, 100-mm target (3)	73 mm × 83 mm, 90% reflective Kodak Gray Card, 8 pulses, PDRIVE = 0 (100%)(3)	415	510	605	counts

Note(s) and/or Footnote(s):

1. Value is factory adjusted to meet the Prox count specification. Considerable variation (relative to the typical value) is possible after adjustment.
2. Proximity offset is the sum of optical and electrical offsets, and will change from one design implementation (or test system) to another. 100% tested.
3. Application design must use correct electrical schematic to ensure proper offset results. Refer to application guide and guidance for proper circuit.

Figure 12:
IR LED Characteristics, V_{DD} = 3 V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_F	Forward Voltage	I_F = 20 mA		1.4	1.5	V
V_R	Reverse Voltage	I_R = 10 µA	5			V
P_O	Radiant Power	I_F = 20 mA	4.5			mW
λ_p	Peak Wavelength	I_F = 20 mA		850		nm
Δ_λ	Spectral Radiation Bandwidth	I_F = 20 mA		40		nm
T_R, T_F	Optical Rise, r Fall Time	I_F = 100 mA, T_W = 125 ns, duty cycle = 25%		20	40	ns

Figure 13:
Wait Characteristics, V_{DD} = 3 V, T_A = 25°C, WEN = 1 (unless otherwise noted)

Parameter	Conditions	Channel	Min	Typ	Max	Units
Wait step size	WTIME = 0xFF		2.25	2.38	2.53	ms

Timing Characteristics

The timing characteristics of TMD3782 are given below.

Figure 14:
AC Electrical Characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

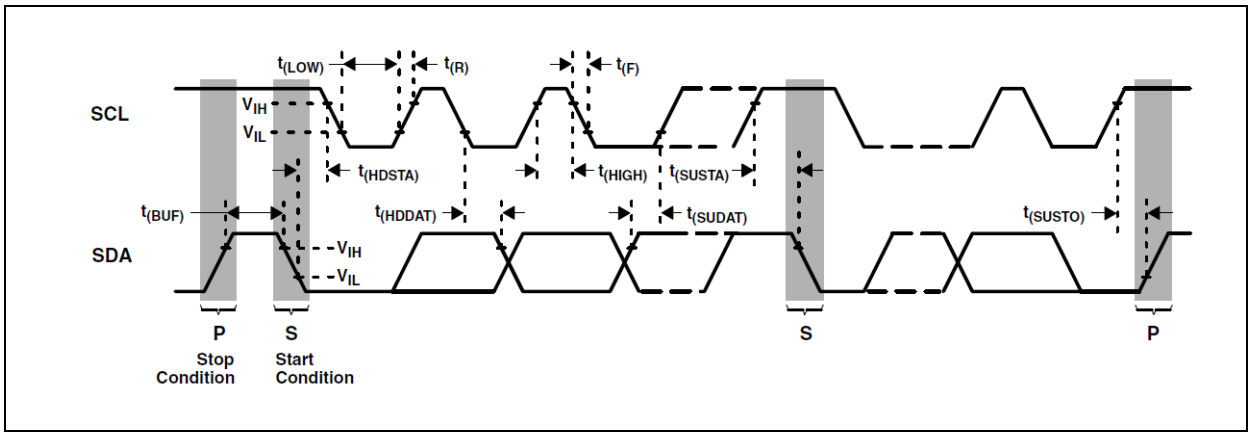
Parameter(1)	Description	Min	Typ	Max	Units
$f_{(SCL)}$	Clock frequency (I^2C only)	0		400	kHz
$t_{(BUF)}$	Bus free time between start and stop condition	1.3			µs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.	0.6			µs
$t_{(SUSTA)}$	Repeated start condition setup time	0.6			µs
$t_{(SUSTO)}$	Stop condition setup time	0.6			µs
$t_{(HDDAT)}$	Data hold time	0			µs
$t_{(SUDAT)}$	Data setup time	100			ns
$t_{(LOW)}$	SCL clock low period	1.3			µs
$t_{(HIGH)}$	SCL clock high period	0.6			µs
t_F	Clock/data fall time			300	ns
t_R	Clock/data rise time			300	ns
C_i	Input pin capacitance			10	pF

Note(s) and/or Footnote(s):

1. Specified by design and characterization; not production tested.

Timing Diagrams

Figure 15:
Parameter Measurement Information



Typical Operating Characteristics

Figure 16:
Spectral Responsivity

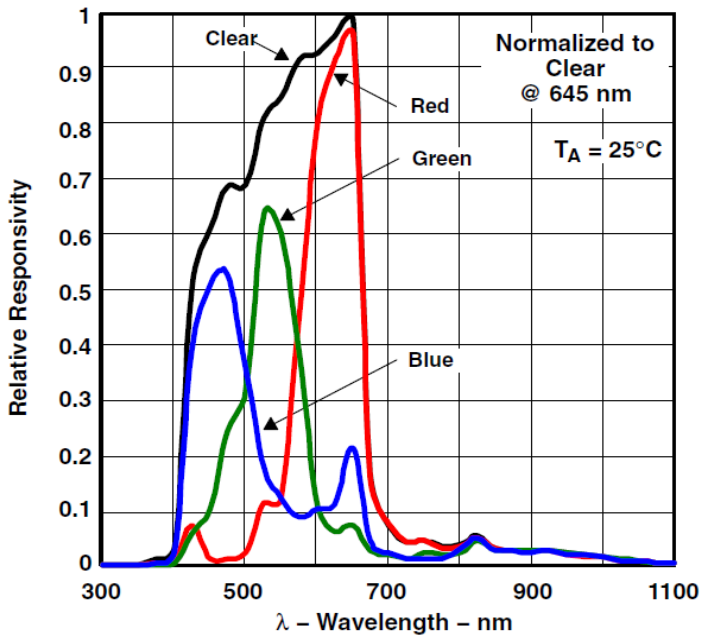


Figure 17:
Normalized I_{DD} vs. V_{DD} and Temperature

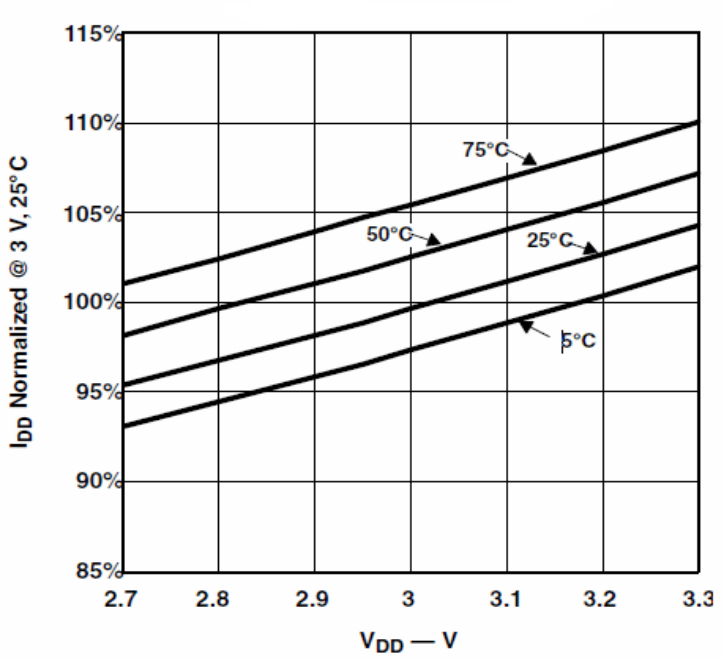


Figure 18:
Typical LDR Current vs. Voltage

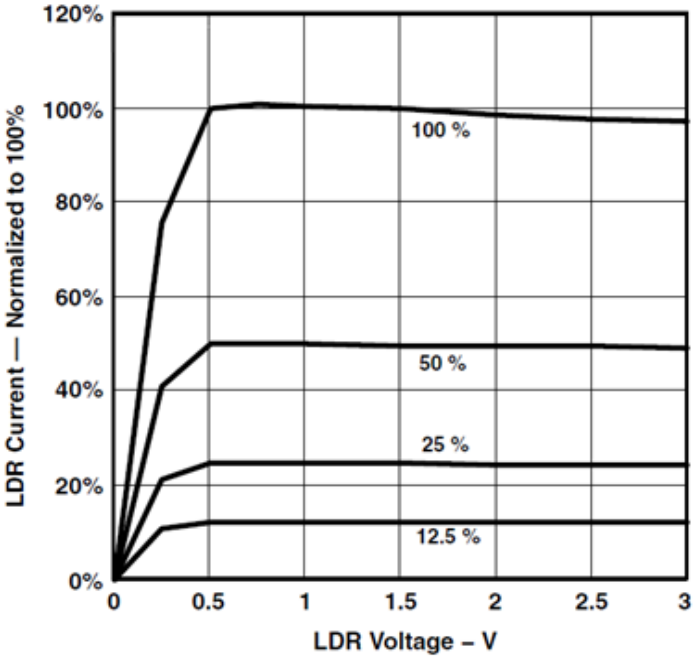


Figure 19:
RGBC Responsivity vs. Angular Displacement

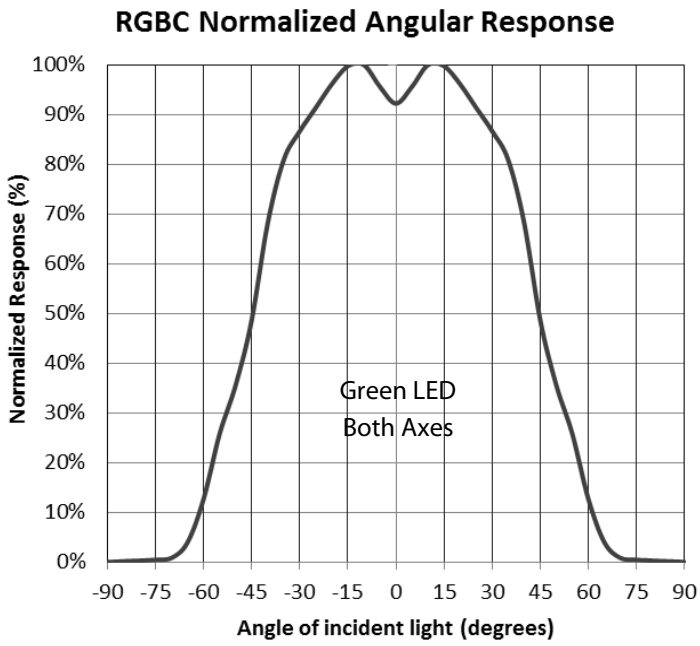


Figure 20:
Proximity Responsivity vs. Angular Displacement

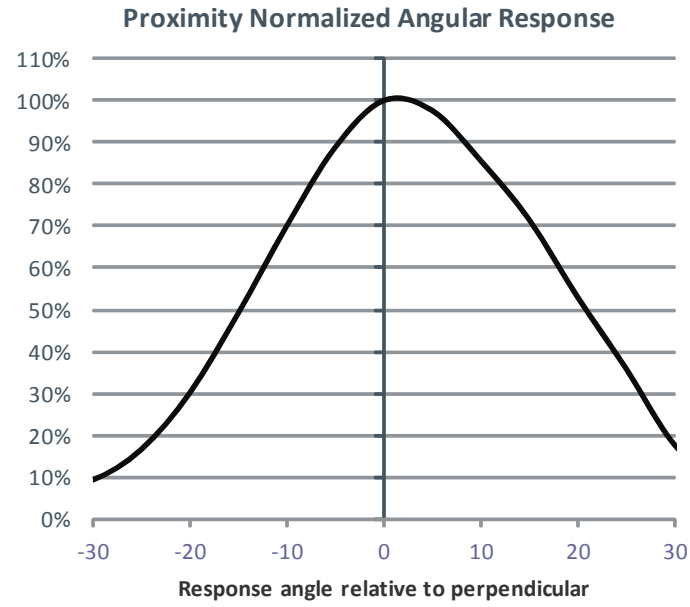
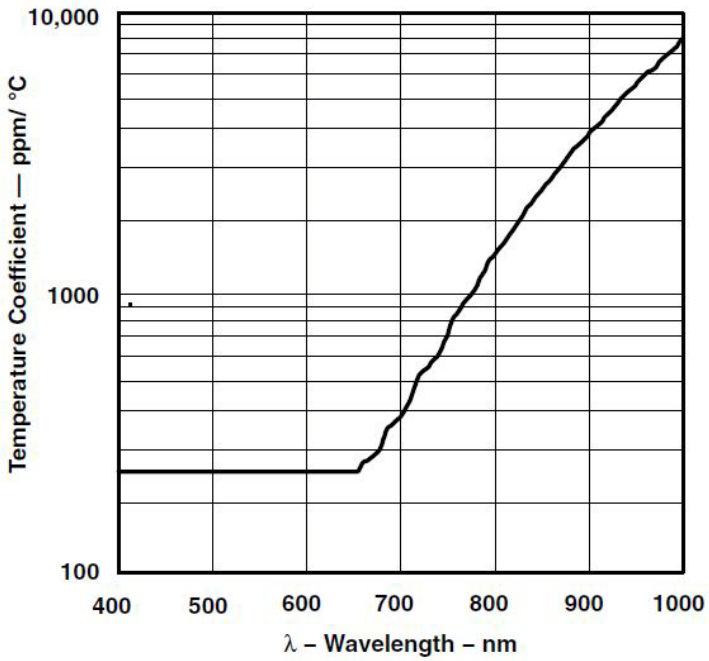


Figure 21:
Responsivity Temperature Coefficient



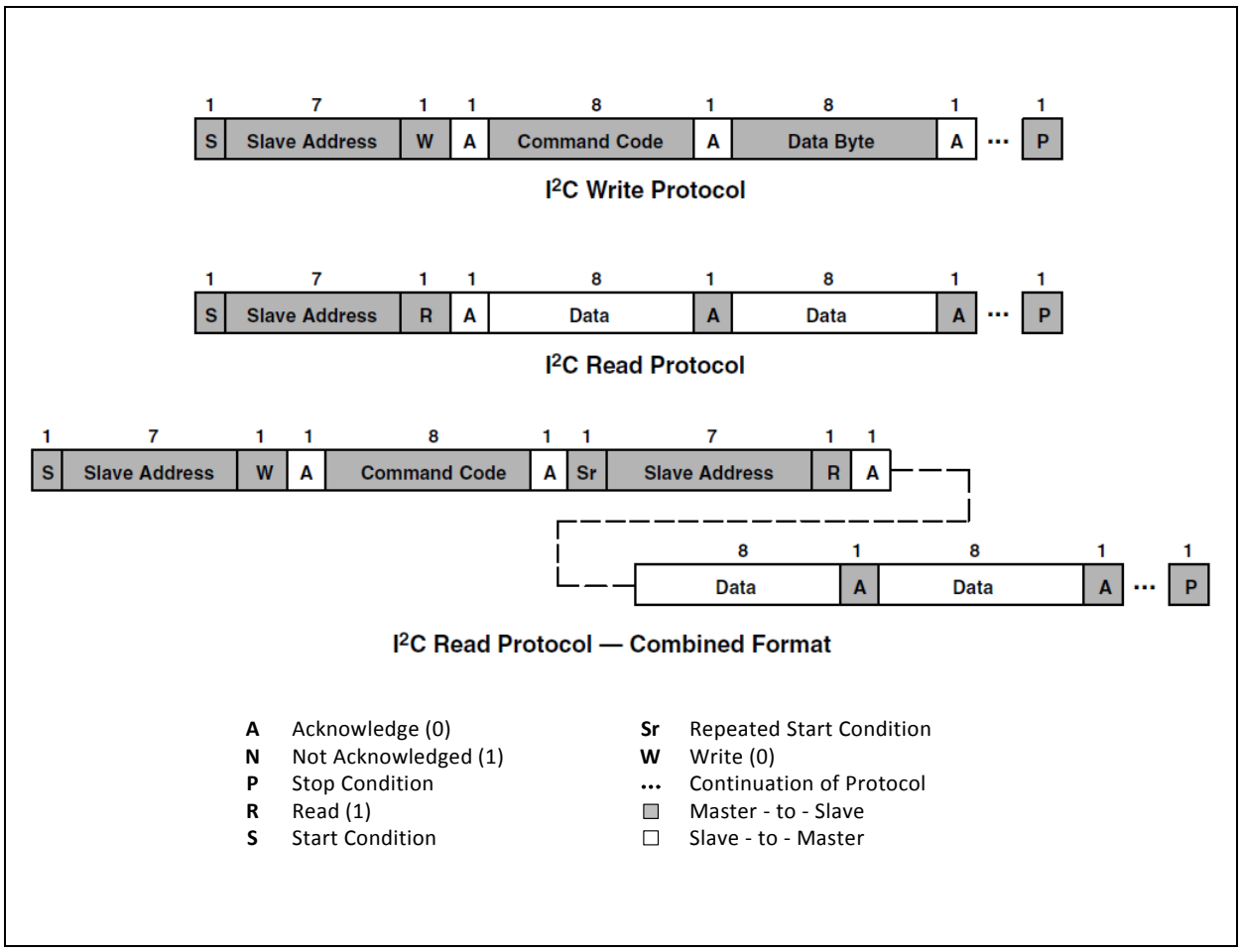
I²C Protocol

Interface and control are accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The devices support the 7-bit I²C addressing protocol.

The I²C standard provides for three types of bus transaction: read, write, and a combined protocol (Figure 22). During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at http://www.I²C-bus.org/references/.

Figure 22:
I²C Write, Read and Combined Protocols



Register Description

The TMD3782 is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Figure 23.

Figure 23:
Register Map

Address	Register Name	R/W	Register Function	Reset Value
-	COMMAND	W	Specified register address	0x00
0x00	ENABLE	R/W	Enables states and interrupts	0x00
0x01	ATIME	R/W	RGBC time	0xFF
0x03	WTIME	R/W	Wait time	0xFF
0x04	AILTL	R/W	Clear interrupt low threshold low byte	0x00
0x05	AILTH	R/W	Clear interrupt low threshold high byte	0x00
0x06	AIHTL	R/W	Clear interrupt high threshold low byte	0x00
0x07	AIHTH	R/W	Clear interrupt high threshold high byte	0x00
0x08	PILTL	R/W	Proximity interrupt low threshold low byte	0x00
0x09	PILTH	R/W	Proximity interrupt low threshold high byte	0x00
0x0A	PIHTL	R/W	Proximity interrupt high threshold low byte	0x00
0x0B	PIHTH	R/W	Proximity interrupt high threshold high byte	0x00
0x0C	PERS	R/W	Interrupt persistence filters	0x00
0x0D	CONFIG	R/W	Configuration	0x00
0x0E	PPULSE	R/W	Proximity pulse count	0x00
0x0F	CONTROL	R/W	Gain control register	0x00
0x11	REVISION	R	Die revision number	Rev.
0x12	ID	R	Device ID	ID
0x13	STATUS	R	Device status	0x00
0x14	CDATA	R	Clear ADC low data register	0x00
0x15	CDATAH	R	Clear ADC high data register	0x00
0x16	RDATA	R	Red ADC low data register	0x00
0x17	RDATAH	R	Red ADC high data register	0x00
0x18	GDATA	R	Green ADC low data register	0x00

Address	Register Name	R/W	Register Function	Reset Value
0x19	GDATAH	R	Green ADC high data register	0x00
0x1A	BDATA	R	Blue ADC low data register	0x00
0x1B	BDATAH	R	Blue ADC high data register	0x00
0x1C	PDATA	R	Proximity ADC low data register	0x00
0x1D	PDATAH	R	Proximity ADC high data register	0x00

The mechanics of accessing a specific register depends on the specific protocol used. In general, the COMMAND register is written first to specify the specific control/status register for following read/write operations.

Command Register

The Command Register specifies the address of the target register for future write and read operations, and is used to clear interrupt sources.

Figure 24:
Command Register

7	6	5	4	3	2	1	0
COMMAND	TYPE		ADD				

Fields	Bits	Description	
COMMAND	7	Select Command Register. Must write as 1 when addressing COMMAND register.	
TYPE	6:5	Selects type of transaction to follow in subsequent data transfers:	
		FIELD VALUE	**TRANSACTION TYPE**
		00	Repeated byte protocol transaction
		01	Auto-increment protocol transaction
		10	Reserved — Do not use
		11	Special function — See description below
		Byte protocol will repeatedly read the same register with each data access. Block protocol will provide auto-increment function to read successive bytes.	

<table>
<tr><th>Fields</th><th>Bits</th><th colspan="2">Description</th></tr>
<tr><td rowspan="8">ADD</td><td rowspan="8">4:0</td><td colspan="2">Address field/special function field. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control−status−register for following write and read transactions. The field values listed below apply only to special function commands:</td></tr>
<tr><td>FIELD VALUE</td><td>SPECIAL FUNCTION</td></tr>
<tr><td>00000</td><td>Normal —no action</td></tr>
<tr><td>00101</td><td>Proximity interrupt clear</td></tr>
<tr><td>00110</td><td>Clear channel interrupt clear</td></tr>
<tr><td>00111</td><td>Proximity and Clear interrupt clear</td></tr>
<tr><td>other</td><td>Reserved — Do not write</td></tr>
<tr><td colspan="2">Clear channel/Proximity Interrupt Clear. Clears any pending Clear/Proximity interrupt. This special function is self clearing.</td></tr>
</table>

System Timing

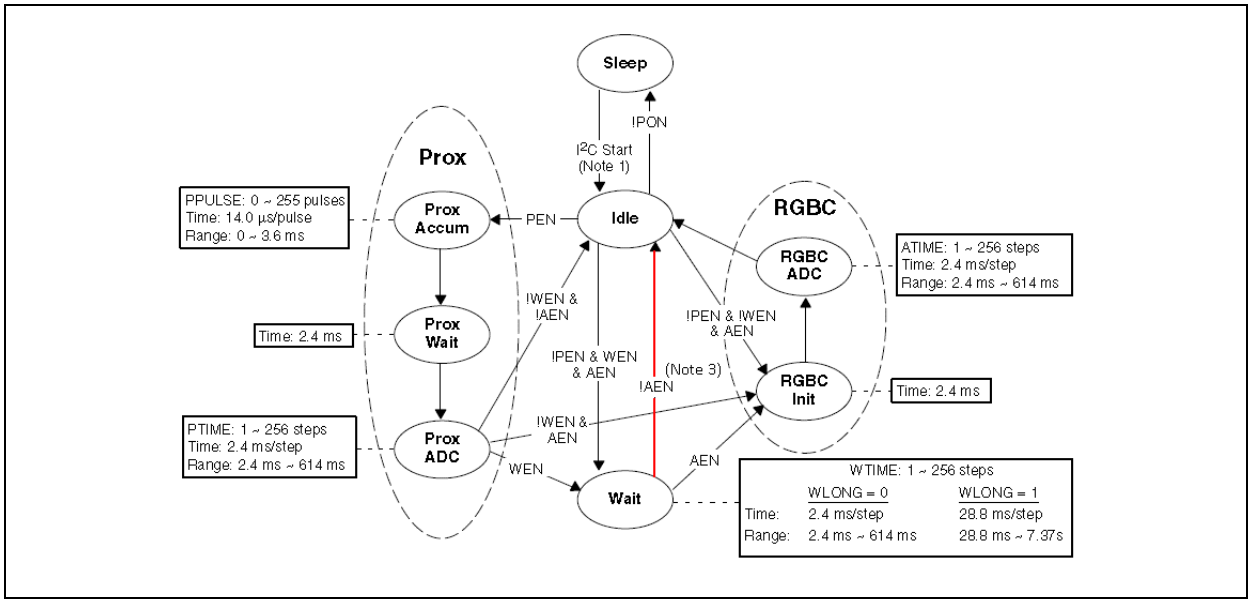
The system state machine shown in Figure 25 provides an overview of the states and state transitions that provide system control of the device. This section highlights the programmable features, which affect the state machine cycle time, and provides details to determine system level timing.

When the proximity detection feature is enabled (PEN), the state machine transitions through the Prox Accum, Prox Wait, and Prox ADC states. The Prox Wait time is a fixed 2.4 ms, whereas the Prox Accum time is determined by the number of proximity LED pulses (PPULSE) and the Prox ADC time is determined by the integration time (PTIME). The formulas to determine the Prox Accum and Prox ADC times are given in the associated boxes in Figure 25. If an interrupt is generated as a result of the proximity cycle, it will be asserted at the end of the Prox ADC state.

When the power management feature is enabled (WEN), the state machine will transition in turn to the Wait state. The wait time is determined by WLONG, which extends normal operation by 12× when asserted, and WTIME. The formula to determine the wait time is given in the box associated with the Wait state in Figure 25.

When the RGBC feature is enabled (AEN), the state machine will transition through the RGBC Init and RGBC ADC states. The RGBC Init state takes 2.4 ms, while the RGBC ADC time is dependent on the integration time (ATIME). The formula to determine RGBC ADC time is given in the associated box in Figure 25. If an interrupt is generated as a result of the RGBC cycle, it will be asserted at the end of the RGBC ADC.

Figure 25:
Enhanced State Machine Diagram



Note(s) and/or Footnote(s):

1. There is a 2.4 ms warm-up delay if PON is enabled. If PON is not enabled, the device will return to the Sleep state as shown.
2. PON, PEN, WEN and AEN are fields in the Enable register (0x00).
3. PON=1, PEN-1, WEN-1, AEN=0 is unsupported and will lead to erroneous proximity readings.

Enable Register (0 x 00)

The Enable Register is used primarily to power the device on and off, and enable functions and interrupts.

Figure 26:
Enable Register

7	6	5	4	3	2	1	0
Reserved		PIEN	AIEN	WEN	PEN	AEN	PON

Field	Bits	Description (Reset value = 0x00)
Reserved	7:6	Reserved. Write as 0.
PIEN	5	Proximity Interrupt Enable. When asserted permits proximity interrupts to be generated, subject to the persist filter.
AIEN	4	Ambient Light Sensing (ALS) Interrupt Enable. When asserted permits ALS interrupts to be generated, subject to the persist filter.
WEN (1), (2)	3	Wait Enable. This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
PEN (1), (2)	2	Proximity enable. This bit activates the proximity function. Writing a 1 enables proximity. Writing a 0 disables proximity.
AEN (1), (2)	1	ADC enable. This bit activates the four-channel (RGBC) ADC. Writing a 1 enables the ADC. Writing a 0 disables the ADC.
PON	0	Power ON. This bit activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator. During reads and writes over the I^2C interface, this bit is temporarily overridden and the oscillator is enabled, independent of the state of PON.

Note(s) and/or Footnote(s):

1. The PON bit must also be set=1 for these functions to operate.
2. WEN=1, PEN=1, AEN=0 is unsupported and will lead to erroneous proximity readings.

RGBC Integration Time Register (0x01)

The RGBC Timing Register controls the internal integration time of the RGBC channel ADCs. Upon power up, the RGBC time register is set to 0xFF.

The maximum (or saturation) count value can be calculated based upon the integration time cycles as follows:

min [CYCLES * 1024, 65535]

Figure 27:
RGBC Integration Time Register

Field	Bits	Description (Reset value = 0xFF)			
		REGISTER VALUE	**CYCLES**	**TIME**	**Max Count**
ATIME	7:0	0xFF	1	2.38 ms	1024
		0xF6	10	24 ms	10240
		0xD6	42	100 ms	43008
		0xC0	64	152 ms	65535
		0x00	256	609 ms	65535

Wait Time Register (0x03)

Wait time is set in 2.38 ms increments unless the WLONG bit is asserted in which case the wait times are 12× longer. WTIME is programmed as a 2's complement number.

Figure 28:
Wait Time Register

Field	Bits	Description (Reset value = 0xFF)			
		REGISTER VALUE	**WAIT TIME**	**TIME (WLONG=0)**	**TIME (WLONG=1)**
WTIME	7:0	0xFF	1	2.38 ms	0.03 s
		0xAB	85	202 ms	2.43 s
		0x00	256	609 ms	7.31 s

Note(s) and/or Footnote(s):

1. The wait time register should be configured before AEN and/or PEN is asserted.

Clear Channel Interrupt Threshold Registers (0x04 - 0x0b)

The Clear Channel Interrupt Threshold Registers provide 16 bit values to be used as the high and low thresholds for comparison to the 16 bit CDATA values. If AIEN (r0x00:b4) is enabled and CDATA is not between AILT and AIHT for the number of consecutive samples specified in APERS (r0x0C) an interrupt is asserted on the interrupt pin.

Figure 29:
Clear Channel Interrupt Threshold Registers

Registers	Address	Bits	Description (Reset value = 0x00)
AILTL	0x04	7:0	ALS low threshold lower byte
AILTH	0x05	7:0	ALS low threshold upper byte
AIHTL	0x06	7:0	ALS high threshold lower byte
AIHTH	0x07	7:0	ALS high threshold upper byte

Proximity Interrupt Threshold Registers (0x04 - 0x0b)

The Proximity Interrupt Threshold Registers provide 16 bit values to be used as the high and low thresholds for comparison to the 16 bit PDATA values. If PIEN (r0x00:b5) is enabled and PDATA is not between PILT and PIHT for the number of consecutive samples specified in PPERS (r0x0C) an interrupt is asserted on the interrupt pin.

Figure 30:
Proximity Interrupt Threshold Registers

Registers	Address	Bits	Description (Reset value = 0x00)
PILTL	0x08	7:0	Proximity low threshold lower byte
PILTH	0x09	7:0	Proximity low threshold upper byte
PIHTL	0x0a	7:0	Proximity high threshold lower byte
PIHTH	0x0b	7:0	Proximity high threshold upper byte

Interrupt Persistence Register (0x0C)

The Interrupt Register controls the interrupt capabilities of the device.

Figure 31:
Interrupt Persistence Register

7	6	5	4	3	2	1	0
PPERS				APERS			

Field	Bits	Description (Reset value = 0x00)	
PPERS	7:4	Proximity interrupt persistence. Controls rate of proximity interrupts to the host processor.	
		FIELD VALUES	**PERSISTENCE**
		0000	Every proximity cycle generates an interrupt
		0001	Any value outside of threshold range
		0010	2 consecutive values out of range
		….	….
		1111	15 consecutive values out of range

Field	Bits	Description (Reset value = 0x00)	
APERS	3:0	Clear channel interrupt persistence. Controls rate of Clear channel interrupts to the host processor.	
		FIELD VALUE	**PERSISTENCE**
		0000	Every RGBC cycle generates an interrupt
		0001	Any value outside of threshold range
		0010	2 consecutive values out of range
		0011	3 consecutive values out of range
		0100	5 consecutive values out of range
		0101	10 consecutive values out of range
		0110	15 consecutive values out of range
		0111	20 consecutive values out of range
		1000	25 consecutive values out of range
		1001	30 consecutive values out of range
		1010	35 consecutive values out of range
		1011	40 consecutive values out of range
		1100	45 consecutive values out of range
		1101	50 consecutive values out of range
		1110	55 consecutive values out of range
		1111	60 consecutive values out of range

Configuration Register (0x0D)

The Configuration Register sets the wait long time.

Figure 32:
Configuration Register

7	6	5	4	3	2	1	0
Reserved						WLONG	Reserved

Field	Bits	Description (Reset value = 0x00)
Reserved	7:2	Reserved. Write as 0.
WLONG	1	Wait Long. When asserted, the wait cycles are increased by a factor 12× from that programmed in the WTIME register.
Reserved	0	Reserved. Write as 0.

Proximity Pulse Count Register (0x0E)

The Proximity Pulse Count Register sets the number of proximity pulses that will be transmitted.

Figure 33:
Proximity Pulse Count Register

Field	Bits	Description (Reset value = 0x00)
PPULSE	7:0	Proximity Pulse Count. Specifies the number of proximity pulses to be generated.

Control Register (0x0F)

The Control Register provides RGBC gain settings and a control for managing the proximity reading in the event the analog circuitry becomes saturated. Bit 5 must be set =1 for proper device operation.

Figure 34:
Control Register

7	6	5	4	3	2	1	0
PDRIVE		Reserved	PSAT	Reserved		AGAIN	

Field	Bits	Description (Reset value = 0x00)	
PDRIVE	7:6	00 = 100% 01 = 50% 10 = 25% 11 = 12.5%	
Reserved	5	Reserved. Must be written = 1	
PSAT	4	0 = PDATA output regardless of ambient light level 1 = PDATA output equal to dark current value if saturated	
Reserved	3:2	Reserved. Write as 00	
AGAIN	1:0	RGBC Gain Control.	
		FIELD VALUE	**RGBC GAIN VALUE**
		00	1X Gain
		01	4X Gain
		10	16X Gain
		11	60X Gain

Revision Register (0x11)

The ID register provides the die revision. This register is a read-only register.

Figure 35:
Revision Register

Field	Bits	Description (Reset value = REV)
RESERVED	7:3	Reserved
REV	2:0	Die revision

ID Register (0x12)

The ID Register provides the value for the part number. This register is a read-only register.

Figure 36:
ID Register

Field	Bits	Description (Reset value = ID)	
ID	7:0	Part number identification.	0x60 = TMD37821 0x69 = TMD37823

Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

Figure 37:
Status Register

7	6	5	4	3	2	1	0
Reserved		PINT	AINT	Reserved		PVALID	AVALID

Field	Bits	Description (Reset value = 0x00)
Reserved	7:6	Reserved.
PINT	5	Proximity Interrupt.
AINT	4	Ambient Light Sensor (ALS) Interrupt.
Reserved	3:2	Reserved.
PVALID	1	Indicates that a proximity cycle has completed since PEN was asserted.
AVALID	0	Indicates that the RGBC cycle has completed since AEN was asserted.

RGBC Data Registers (0x14 - 0x1b)

Clear, red, green, and blue data is stored as 16-bit values. To ensure the data is read correctly, a two-byte read I^2C transaction should be used with a read word protocol bit set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Figure 38:
RGBC Data Registers

Register	Address	Bits	Description (Reset value = 0x00)
CDATAL	0x14	7:0	Clear data low byte
CDATAH	0x15	7:0	Clear data high byte
RDATAL	0x16	7:0	Red data low byte
RDATAH	0x17	7:0	Red data high byte
GDATAL	0x18	7:0	Green data low byte
GDATAH	0x19	7:0	Green data high byte
BDATAL	0x1a	7:0	Blue data low byte
BDATAH	0x1b	7:0	Blue data high byte

Proximity Data Registers (0x1c - 0x1d)

Proximity data is stored as a 16-bit value. To ensure the data is read correctly, a two-byte read I^2C transaction should be used with a read word protocol bit set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Figure 39:
Proximity Data Registers

Register	Address	Bits	Description (Reset value = 0x00)
PDATAL	0x1c	7:0	Proximity data low byte
PDATAH	0x1d	7:0	Proximity data high byte

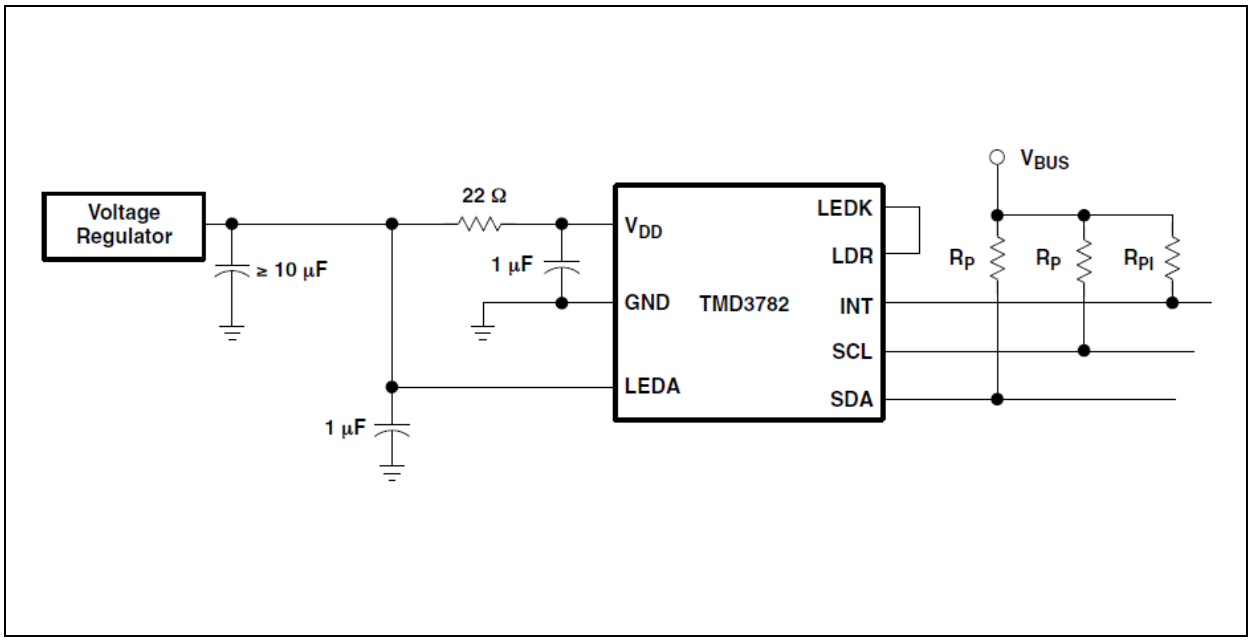
Application Information

In a proximity sensing system, the IR LED can be pulsed by the TMD3782 with more than 100 mA of rapidly switching current, therefore, a few design considerations must be kept in mind to get the best performance. The key goal is to reduce the power supply noise coupled back into the device during the LED pulses. If V_{bat} does not exceed the maximum specified LDR pin voltage (including when the battery is being recharged), LEDA can be directly tied to V_{bat} for best proximity performance.

In many systems, there is a quiet analog supply and a noisy digital supply. By connecting the quiet supply to the V_{DD} pin and the noisy supply to the LED, the key goal can be meet. Place a 1-µF low-ESR decoupling capacitor as close as possible to the V_{DD} pin and another at the LED anode, and a 10 - 22µF bulk capacitor at the output of the LED voltage regulator to supply the 100-mA current surge.

If operating from a single supply, use a 22-Ω resistor in series with the V_{DD} supply line and a 1-µF low ESR capacitor to filter any power supply noise. The previous capacitor placement considerations apply.

Figure 40:
Typical Application Hardware Circuit



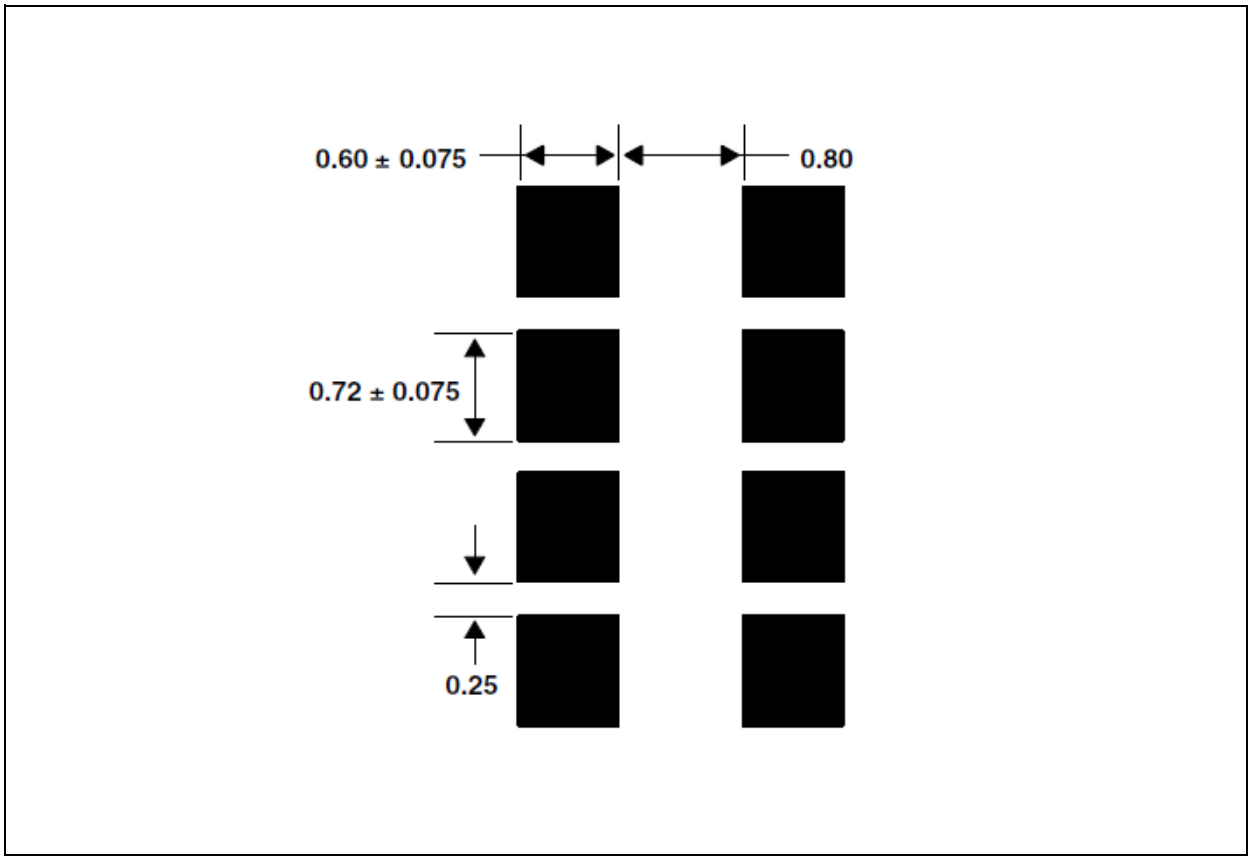
V_{BUS} in the above figure refers to the I²C bus voltage which is either V_{DD} or 1.8 V. Be sure to apply the specified I²C bus voltage shown in the Available Options table for the specific device being used.

The I²C signals and the Interrupt are open-drain outputs and require pull–up resistors. The pull-up resistor (RP) value is a function of the I²C bus speed, the I²C bus voltage, and the capacitive load. The **ams** EVM running at 400 kbps, uses 1.5-kΩ resistors. A 10-kΩ pull-up resistor (RPI) can be used for the interrupt line.

PCB Pad Layout

Suggested PCB pad layout guidelines for the surface mount module are shown. Flash Gold is recommended surface finish for the landing pads.

Figure 41:
Suggested PCB Layout

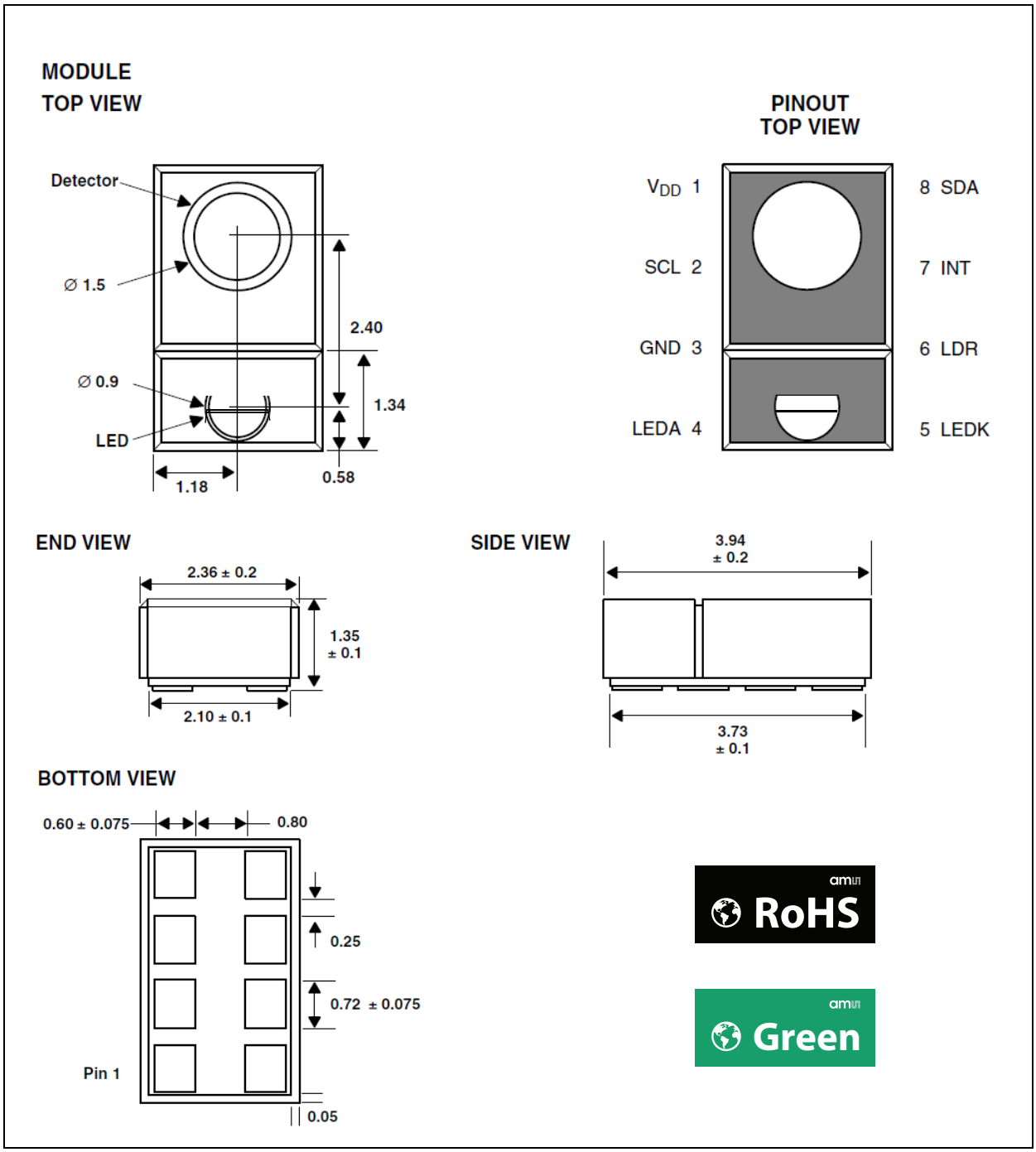


Note(s) and/or Footnote(s):

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

Package Drawings & Markings

Figure 42:
Package Diagrams



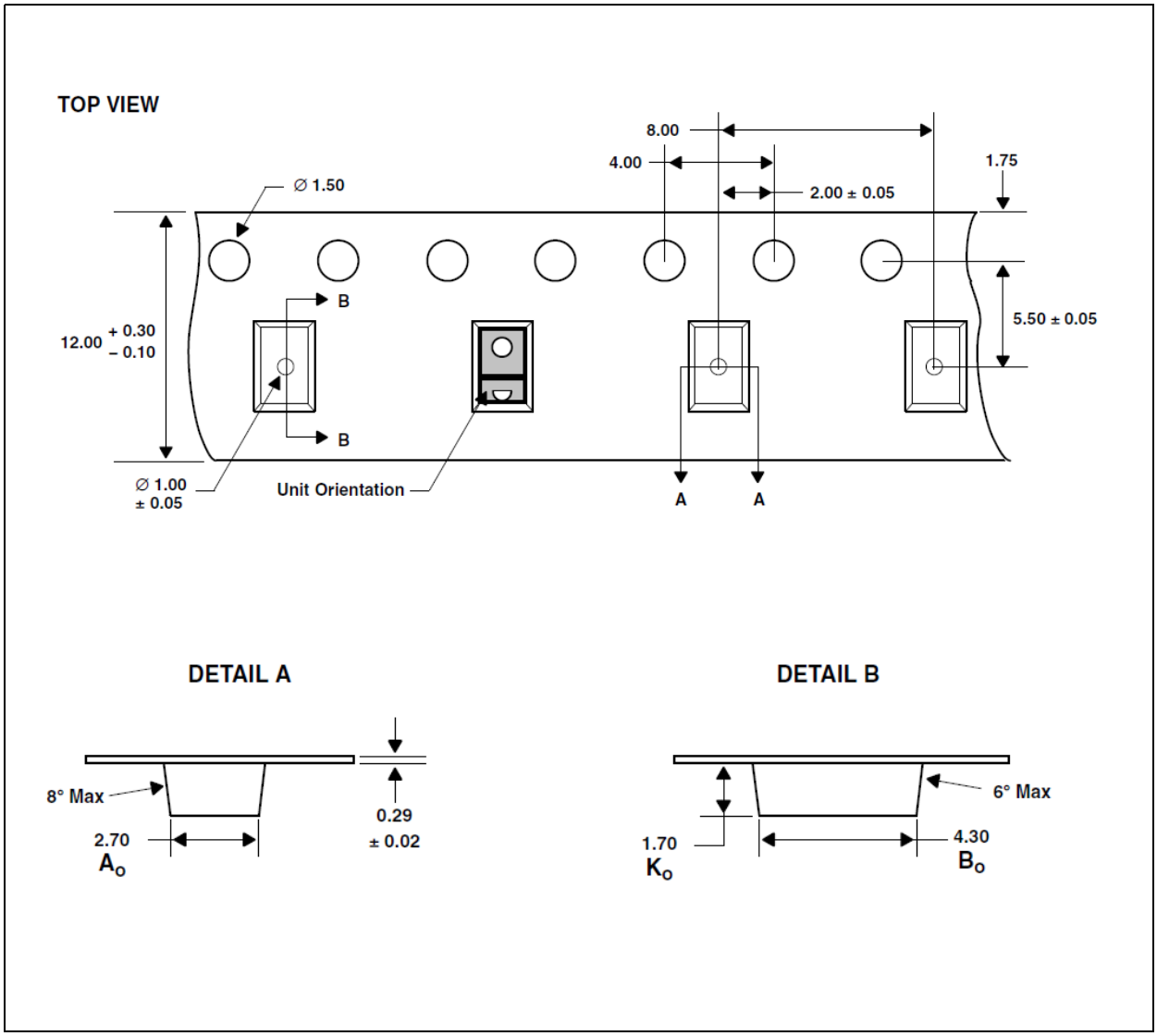
Note(s) and/or Footnote(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ± 0.05 mm unless otherwise noted.
2. Contacts are copper with NiPdAu plating.
3. This package contains no lead (Pb).
4. This drawing is subject to change without notice.

Mechanical Data

The mechanical data of TMD3782 is explained below.

Figure 43:
Carrier Tape and Reel Information



Note(s) and/or Footnote(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing Ao, Bo, and Ko are defined in ANSI EIA Standard 481–B 2001.
4. Each reel is 330 millimeters in diameter and contains 2500 parts.
5. **ams** packaging tape and reel conform to the requirements of EIA Standard 481–B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

Soldering and Storage Information

Soldering Information

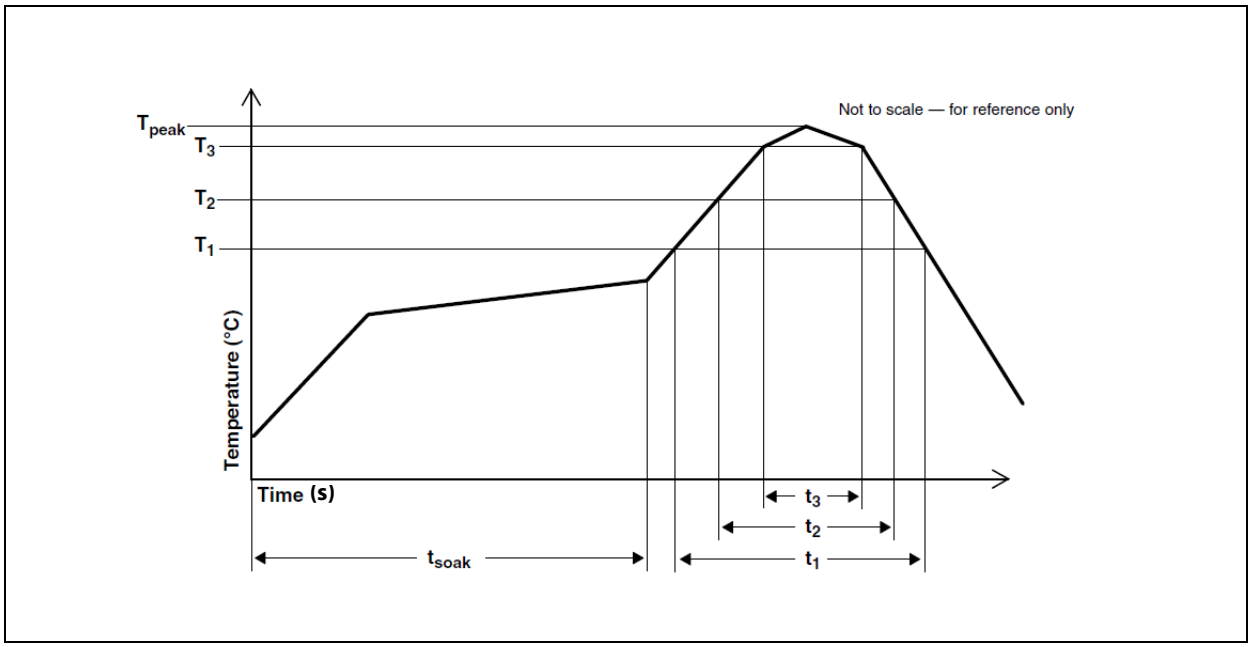
The package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 44:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217 °C (T1)	t_1	Max 60 s
Time above 230 °C (T2)	t_2	Max 50 s
Time above T_{peak} - 10 °C (T3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260 °C
Temperature gradient in cooling		Max -5 °C/s

Figure 45:
Solder Reflow Profile Graph



Storage Information

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping.

Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

Shelf Life: 12 months

Ambient Temperature: < 40°C

Relative Humidity: < 90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

Floor Life: 168 hours

Ambient Temperature: < 30°C

Relative Humidity: < 60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Ordering & Contact Information

Figure 46:
Ordering Information

Ordering Code	Address	Interface	Delivery Form
TMD37821	0x39	I^2C $V_{bus} = V_{DD}$ Interface	Module-8
TMD37823	0x39	I^2C bus = 1.8V Interface	Module-8
TMD37825 (1)	0x29	I^2C $V_{bus} = V_{DD}$ Interface	Module-8
TMD37827 (1)	0x29	I^2C bus = 1.8V Interface	Module-8

Note(s) and/or Footnote(s):

1. Contact **ams** for availability.

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Tobelbaderstrasse 30
8141 Unterpremstaetten
Austria, Europe

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Document Status	Product Status	Definition
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Revision Information

Changes from 3-01 (2014-Oct-21) to current revision 3-02 (2015-Sep-11)	Page
Updated Figure 11	9

Note(s) and/or Footnote(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide